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Jpn. J. Appl. Phys. **52** (2013) 06GC02

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Japanese Journal of Applied Physics **52** (2013) 06GC02 **REGULAR PAPER**
http://dx.doi.org/**10.7567/JJAP.52.06GC02**

# Mask Effects on Resist Variability in Extreme Ultraviolet Lithography

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Received December 4, 2012; revised January 28, 2013; accepted February 1, 2013; published online June 20, 2013

Resist variability is one of the challenges that must to be solved in extreme UV lithography. One of the root causes of the resist roughness are the mask contributions. Three different effects may plays a non-negligible role: mask pattern roughness transfer — or mask line edge roughness, speckle effects caused by mask surface roughness, and mask layout which causes local flare amplification at wafer level. In this paper, mask contributions to the pattern variability are individually assessed experimentally and via stochastic simulations for both lines/spaces and contact holes. It was found that the predominant effect is the mask layout, while the speckle contribution is barely detectable.
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## 1. Introduction

Process variability in today's lithography might be a showstopper for extreme UV (EUV) lithography for the 22 nm technology node and beyond. At these feature sizes, electrical devices are influenced by quantum effects and thus have to face the discrete behavior of light and matter. Lithography uncertainties such as photon/acid shot noise, photomask roughness, diffusion and thermal processes of the photoresist material, fractal behavior of chemical species and polymer deprotection noise contribute to the formation of resist line edge roughness (LER) and contact hole (CH) variability in terms of local critical dimension uniformity (LCDU).

EUV masks do contribute to the final resist variability in different ways. The first is caused by LER and LCDU of the mask pattern itself. The mask pattern is created using electron-beam lithography, followed by different etch steps, both characterized by randomness which generate roughness in the mask pattern.[1–14] The second effect, called speckle, is generated by the mask surface roughness (MSR),[15–18] again due to the mask fabrication process. The surface roughness of EUV masks is translated in a phase mismatch of the reflected photons. This effect leads to speckle pattern formation[19–25] which causes intensity undulations at wafer level. This intensity variation is then translated into edge placement uncertainty of resist features. The third effect is related to the mask layout, in particular to the percentage of absorber tiling nearby the pattern to be transferred into the resist. The flare percentage at wafer level is directly related to the absorber coverage present at mask level, representing a DC light background which worsen the aerial image quality.[26–29]

In the next three paragraphs, each of these mask effects are quantified with both experimental results and stochastic simulations[30] performed with the lithography simulator PROLITH.[31] Resist LER and LCDU are reported normalized due to the high dependency of these numbers from critical dimension-scanning electron microscopy (CD-SEM) metrology.[32]

## 2. Mask Pattern Roughness

As reported in Refs. 3 and 11, mask pattern impact on printed structures depends on the optical system and its high-frequency cut-off. In case of the pre-production EUV exposure tool with $NA = 0.25$ projection optics (ASML NXE:3100) and conventional illumination, frequencies higher than:

$$f_{\text{cut-off}} = \frac{NA}{\lambda}(1 + \sigma_{\text{out}}) = \frac{0.25}{13.5}(1 + 0.81) = 34\,\mu\text{m}^{-1} = \frac{1}{29.4\,\text{nm}}, \qquad (1)$$

where $NA$ is the numerical aperture of the system, $\lambda$ is the wavelength, and $\sigma_{\text{out}}$ is the coherence factor of the conventional illumination are not transmitted. Therefore, only mask pattern roughness frequencies lower than $f_{\text{cut-off}}$ are transmitted at wafer level, and its impact is be visible mostly in the low-frequency (LF) region.

Following the methodology already reported in Ref. 3, mask pattern roughness was imported into PROLITH through edge detection of the CD-SEM image in Fig. 1(b). This image was generated by stitching six CD-SEM images taken along the same mask lines with a symmetric field of view [FoV; Fig. 1(a)] of $0.36 \times 0.36\,\mu\text{m}^2$ and then compressed in the $Y$-direction (along the lines) in order to obtain an asymmetric FoV[32] of $0.36 \times 2.16\,\mu\text{m}^2$ (dimensions reported at wafer level). This procedure was necessary to match the metrology at wafer level, where CD-SEM asymmetric FoV is commonly used to capture LF roughness [Fig. 1(c)], in agreement with the ITRS specifications.[33] Such metrology allowed us to detect a broader roughness frequency spectrum, maximizing the mask LER impact on resist pattern.

To evaluate the mask impact on resist LER, three different simulations were run on 27 nm half-pitch (hp) lines/spaces (L/S):

- Continuum simulations with real mask profile [Fig. 2(a)] to evaluate the mask pattern roughness transfer at wafer level

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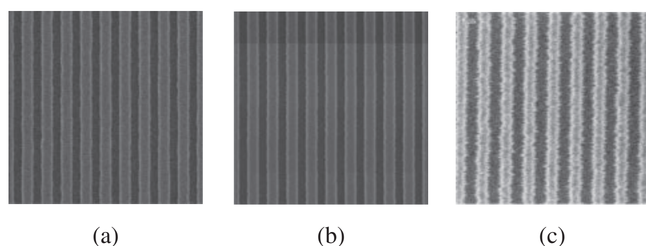
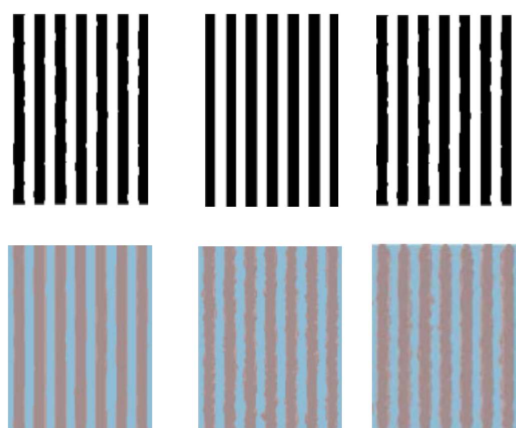
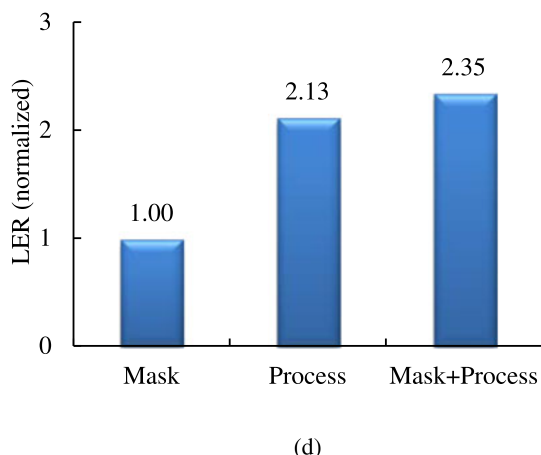



**Fig. 1.** Top-down CD-SEM images of 27 nm half-pitch lines/spaces of the mask (a) with symmetric FoV (b) with asymmetric FoV created by stitching six symmetric images followed by a compression in the $Y$-direction, and (c) of the resist with asymmetric FoV.



(a) (b) (c)




(d)

**Fig. 2.** (Color online) PROLITH mask (upper column) and resist profiles (local column) in (a) continuum simulation mode with real mask profile, (b) stochastic simulation mode with ideal mask profile (mask LER = 0), and (c) stochastic simulation mode with real mask profile. (d) Resist LER (normalized) for the three different cases.

- Stochastic simulations (100 runs) with ideal mask profile [Fig. 2(b)] to evaluate the stochastic effects of the lithography process on the resist variability
- Stochastic simulations (100 runs) with real mask profile [Fig. 2(c)] for the overall impact (mask and process) on the resist roughness

As reported in the graph of Fig. 2(d), even in continuum simulation mode, the mask pattern LER is transferred on the resist pattern; however, once all the stochastic processes are considered (shot noises, acid diffusion, deprotection/reaction noise, etc.), the mask pattern LER contribute only to roughly 10% of the overall resist roughness.

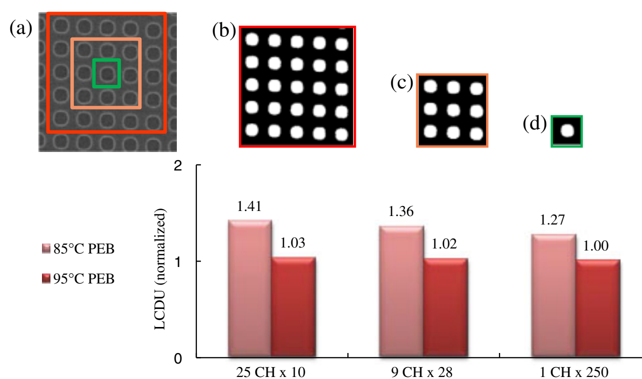



**Fig. 3.** (Color online) (a) Top-down CD-SEM image of 30 nm hp CH on mask. (b), (c), and (d) are the mask layouts implemented in PROLITH to simulate respectively 25 × 10, 9 × 28, and 1 × 250 CH, respectively. The graph represents the LCDU (normalized) of the three different mask layouts for two PEB temperatures (85 and 95 °C).

The mask contribution in the case of CH was estimated with a similar approach: in the first stochastic simulation, 25 different mask CHs [Fig. 3(a) in red and in Fig. 3(b)] were simulated 10 times. The same simulation was then repeated for a mask with only 9 different CHs [28 times, Fig. 3(a) in pink and Fig. 3(c)] and, as an ideal case, a mask populated by only 1 CH exposed 250 times [Fig. 3(a) in green and Fig. 3(d)] was run. The same approach was repeated for two post exposure bake (PEB) temperatures (85 and 95 °C). The results are reported in the bar graph of Fig. 3: the ideal case, with 250 equal CHs on mask (mask LCDU = 0) shows the lowest LCDU values for both PEBs. Comparing to the ideal case (mask LCDU = 0), in the other two cases is possible to notice a gradual increase of resist CH variability, mostly due to CH area variability from contact to contact. During exposure, this variability is translated in photon flux variability, which increases the photon distribution uncertainty at wafer level.

The LCDU values are generally higher with 85 °C PEB temperature. This difference can be explained considering that both acid diffusion and exposure dose change by varying the PEB temperature: for a higher PEB temperature, acid diffusion increases, thereby decreasing the exposure dose. The difference in dose is however only 14% (17.7 $mJ/cm^2$ for 85 °C and 15.3 $mJ/cm^2$ for 95 °C), with a photon shot noise[34] uncertainty difference of less than 2%. We can conclude that the main LCDU variation between different PEB temperatures is caused by a closer value of the acid diffusion to the optimum[34] for 95 °C PEB (which is also the recommended value for the considered resist).

Intuitively, the mask effect is higher for lower PEB temperature, where the acid diffusion is shorter, and the mask variability is less smoothened during the diffusion process. For the considered case, an overall limited impact of less than 10% was found.

## 3. Mask Surface Roughness

In this paragraph we complete the evaluation of the speckle effect on resist pattern caused by the MSR. In collaboration

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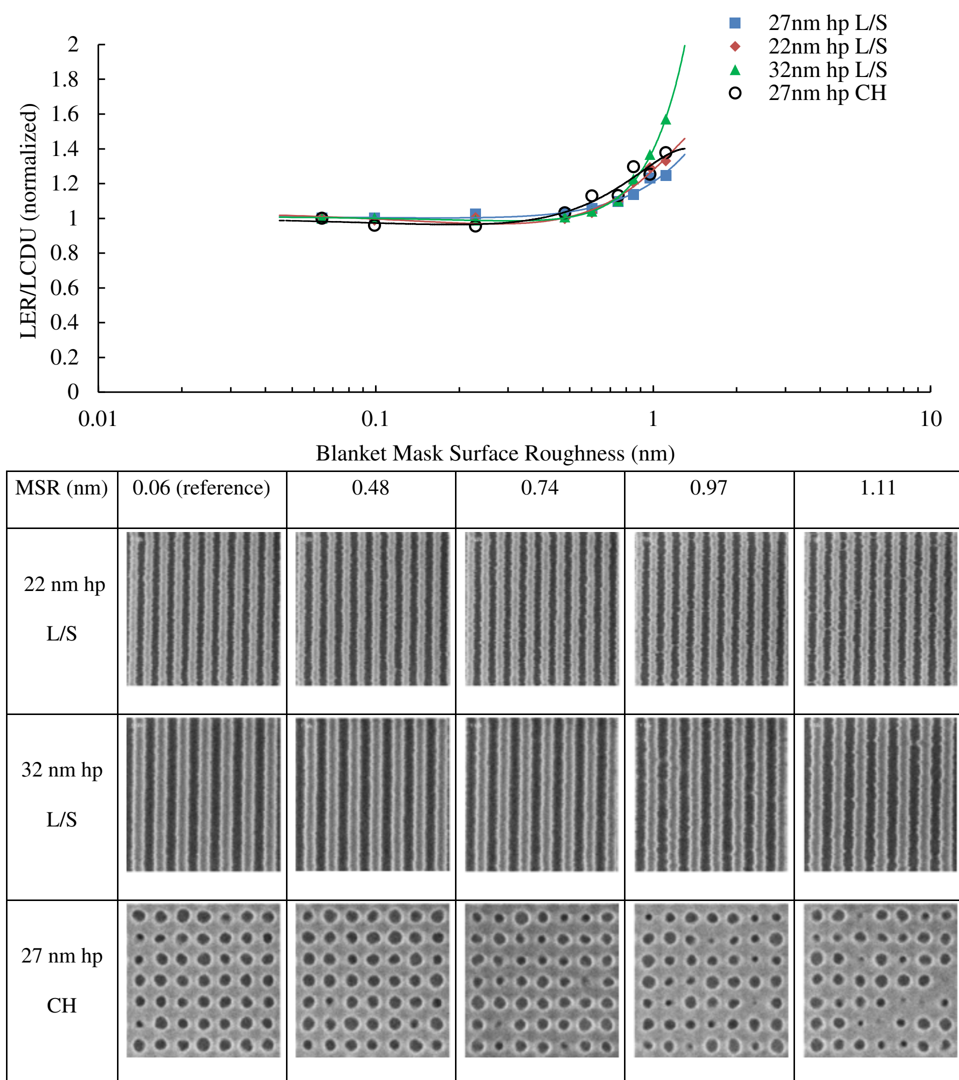


**Fig. 4.** (Color online) Top: LER and LCDU (normalized) for 27 (blue line), 22 (red line), 32 (green line) nm hp L/S and 27 nm hp CH (black empty dots). Bottom: Top-down CD-SEM images for 22 and 32 nm hp L/S and 27 nm hp CH exposed at different MSR (speckle) levels.

with Intel, Sematech, and Lawrence Berkeley National Lab, a special mask with a surface roughness gradient was prepared. AFM measurements performed along the blanket show incremental MSR roughness varied from more than 1 nm (roughest area) to 0.06 nm for the reference case.[15,17,18,24] For the methodology, metrology and the experimental details of the exposures we refer to Refs. 18 and 24.

In the graph of Fig. 4, experimental results previously obtained at 27 (blue curve) and 22 nm (red curve) hp L/S[24] on standard EUV resist (exposure dose: $\sim$15 mJ/cm$^2$) are compared with a slower but more performing material supplied by JSR used to print on a more relaxed pitch (32 nm hp, green curve). The last exposure was performed to understand whether the speckle contribution to LER would have been detected at lower MSR on a more performing resist in terms of LER (a factor of 2 lower compared to the 22 and the 27 nm case), as reported in literature.[15,17)]

Despite the lower LER value for the JSR material at 32 nm hp, the speckle contribution do appear again only for MSR $>$ 0.5 nm rms, a value well above compared to what predicted by previous simulations.[15,17]

To complete the speckle assessment, 27 nm hp CHs were also analyzed. As for the L/S cases, the CH LCDU increases only for MSR $>$ 0.5 nm rms, well overlapping the L/S behavior.

From these results, we can conclude that very limited resist variability (below 5%, comparable with the metrology noise) is caused by the speckle.

## 4. Mask Layout

Masks can have a very broad absorber surface coverage depending on the layout to be transferred into the resist. Mask with high absorber coverage (i.e., CH layouts) are defined as dark-field masks; on the contrary bright-field masks (i.e., gate layouts) have a lower % of absorber. The absorber coverage determines the level of DC flare (background scattered light) at wafer level. This DC component has mainly the effect of decreasing the exposure dose, and worsens the aerial image quality, resulting in higher LER. To assess the mask layout contribution to the resist LER, 28 nm hp L/S were exposed on five different resists supplied by TOK with three layouts characterized by diverse absorber coverage. The absorber coverage was varied by changing

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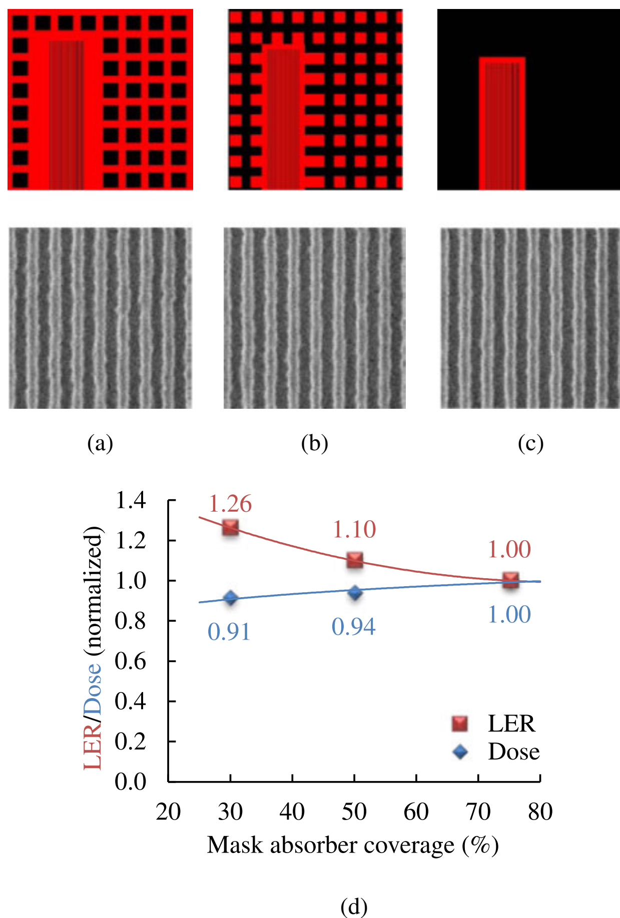


**Fig. 5.** (Color online) In the top row mask layout screenshots of 28 nm hp L/S are reported for (a) 30% absorber coverage (bright field), (b) 50% absorber coverage, and (c) 75% absorber coverage (dark field). In the bottom row, top-down CD-SEM images of 28 nm hp L/S features printed on resist are reported for the different absorber coverage levels. (d) Resist LER (red) and exposure dose (blue) for the three different cases are reported (normalized) upon mask absorber coverage.

the absorber tiling around the features to be printed (Fig. 5 top row).

Already observing the CD-SEM images of the 28 nm hp L/S captured for different absorber coverage levels (Fig. 5, bottom row), it is possible to notice a substantial improvement of the line profiles moving from bright to dark field. In the graph of Fig. 5(d), LER average for the different resists (in red) is plotted upon absorber coverage (%). 26% more roughness was quantified moving from 75 to 30% absorber tiling. This effect can be only partially explained considering the different exposure doses (blue trend) used to target 28 nm CD L/S. The dose gap between bright and dark field is less than 10%, corresponding to only 5% photon shot noise difference. Local flare change is the responsible for the remaining LER discrepancy.

Although hardly tunable, mask layout and the respective absorber coverage level play a non-negligible role in terms of resist performance, and should be taken in consideration for eventual resist LER mitigation.

## 5. Conclusions

In this paper mask contributions on resist roughness were quantified for EUV lithography by means of both stochastic simulations and experimental results. Three effects were identified as possible root causes of pattern LER at wafer level for the sub-32 nm technology node. The first effect is the variability of the mask pattern itself, which is transferred at wafer level due to the high resolution of the EUV exposure tools. Most of the mask pattern variability is translated in LF roughness in case of L/S, or local photon flux variations in case of CH. However, for both the cases, an impact of 10% or less on the overall resist variability is expected with the current state-of-the-art EUV masks.

Speckle effects on LER and LCDU caused by mask surface roughness were also considered. The results qualitatively confirmed the predictions made in previous works. However, the quantitative impact of the speckle effect is less than expected. Previous simulations predicted a non-negligible speckle contribution to the photoresist variability for mask surface roughness higher than 0.05 nm rms, but in our experiments the photoresist performance started degrading for mask surface roughness values 10 times higher, resulting in less than 5% contribution to the overall resist variability.

The third effect is related to the local flare level at wafer level, caused by different mask layouts. Printing the same type of features with different absorber coverage is translated in diverse resist performance. In the cases analyzed in this work, 26% LER reduction was found by increasing the absorber tiling from 30% (bright field mask) to 75% (dark field mask). The effect can be only partially explained by the exposure dose gain, and the resulting shot noise improvement.

Considering the main challenges which EUV lithography must still overcome in order to be considered viable for high volume manufacturing, this work reveals that further improvement of existing mask manufacturing processes—pattern and surface roughness—will not likely be translated in photoresist pattern variability improvement. However, substantial progress can be made if mask layouts are considered as another limiting factor of the resist performance.

## Acknowledgements

The authors would like to thank Rudi De Ruyter (IMEC) for the mask layout designs, Takehito Seo (TOK), Kenji Hoshiko and Yusuke Anno (JSR) for supplying resist materials and supporting our exposures.


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